The ULN2803A is a high-voltage, high-current Darlington transistor array. The device consists of eight npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>−40°C to 85°C</td>
<td>PDIP (N)</td>
<td>Tube of 20</td>
<td>ULN2803AN</td>
</tr>
<tr>
<td></td>
<td>SOIC (DW)</td>
<td>Tube of 40</td>
<td>ULN2803ADW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reel of 2000</td>
<td>ULN2803ADWR</td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
logic diagram

schematic (each Darlington pair)
absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-emitter voltage</td>
<td>VCE = 50 V, See Figure 1</td>
<td>50</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Input voltage (see Note 1)</td>
<td>VCE = 50 V, TAI = 70°C, See Figure 2</td>
<td>50</td>
<td>65</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Continuous collector current</td>
<td>VCE = 2 V, See Figure 4</td>
<td></td>
<td>0.93</td>
<td>1.35</td>
<td>mA</td>
</tr>
<tr>
<td>Total substrate-terminal current</td>
<td></td>
<td>2.4</td>
<td>1.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Package thermal impedance, θJA</td>
<td>DW package</td>
<td>73.14</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>N package</td>
<td>62.66</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating virtual junction temperature, TJ</td>
<td></td>
<td></td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range, Tstg</td>
<td></td>
<td></td>
<td></td>
<td>−25</td>
<td>°C</td>
</tr>
</tbody>
</table>

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.

2. Maximum power dissipation is a function of TJ(max), θJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) − TA)/θJA. Operating at the absolute maximum TJ of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICEX</td>
<td>Collector cutoff current</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>II(off)</td>
<td>Off-state input current</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>II(on)</td>
<td>Input current</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>V(on)</td>
<td>On-state input voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VCE(sat)</td>
<td>Collector-emitter saturation voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IR</td>
<td>Clamp diode reverse current</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>VF</td>
<td>Clamp diode forward voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Ci</td>
<td>Input capacitance</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

switching characteristics at 25°C free-air temperature

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH</td>
<td>Propagation delay time, low- to high-level output</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tPHL</td>
<td>Propagation delay time, high- to low-level output</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VOH</td>
<td>High-level output voltage after switching</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

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3
PARAMETER MEASUREMENT INFORMATION

Figure 1. $I_{CEX}$ Test Circuit

Figure 2. $I_{I(off)}$ Test Circuit

Figure 3. $I_{I(on)}$ Test Circuit

Figure 4. $V_{I(on)}$ Test Circuit

Figure 5. $h_{FE}, V_{CE(sat)}$ Test Circuit

Figure 6. $I_R$ Test Circuit
PARAMETER MEASUREMENT INFORMATION

Figure 7. $V_F$ Test Circuit

NOTES:  
A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O = 50 \, \Omega$.
B. $C_L$ includes probe and jig capacitance.
C. $V_{IH} = 3 \, V$

Figure 8. Propagation Delay Times
PARAMETER MEASUREMENT INFORMATION

NOTES:
A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_0 = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V

Figure 9. Latch-Up Test
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULN2803ADW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td><img src="samples.png" alt="Samples" /></td>
</tr>
<tr>
<td>ULN2803ADWG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td><img src="samples.png" alt="Samples" /></td>
</tr>
<tr>
<td>ULN2803ADWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td><img src="samples.png" alt="Samples" /></td>
</tr>
<tr>
<td>ULN2803ADWRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td><img src="samples.png" alt="Samples" /></td>
</tr>
<tr>
<td>ULN2803AN</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>18</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-40 to 85</td>
<td>ULN2803AN</td>
<td><img src="samples.png" alt="Samples" /></td>
</tr>
<tr>
<td>ULN2803ANE4</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>18</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-40 to 85</td>
<td>ULN2803AN</td>
<td><img src="samples.png" alt="Samples" /></td>
</tr>
</tbody>
</table>

### Footnotes:
1. The marketing status values are defined as follows:
   - **ACTIVE**: Product device recommended for new designs.
   - **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
   - **OBsolete**: TI has discontinued the production of the device.

2. **Eco Plan** - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
   - **TBD**: The Pb-Free/Green conversion plan has not been defined.
   - **Pb-Free (RoHS)**: TI's terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
   - **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
   - **Green (RoHS & no Sb/Br)**: TI defines “Green” to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

3. **MSL, Peak Temp.** – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.
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# TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULN2803ADWR</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>10.9</td>
<td>12.0</td>
<td>2.7</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
</tr>
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</table>

*All dimensions are nominal.*
TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULN2803ADWR</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>2000</td>
<td>370.0</td>
<td>355.0</td>
<td>55.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:  
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).  
D. Falls within JEDEC MS–013 variation AB.
NOTES:  
A. All linear dimensions are in millimeters. 
B. This drawing is subject to change without notice. 
C. Refer to IPC7351 for alternate board design. 
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525. 
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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